IN THE SPECIFICATION

Please amend the appropriate paragraphs of specification in accordance with proposed changes as outlined hereinbelow:

Please amend the paragraph bridging pages 20 and 21, from line 20 on page 20 to line 10 on page 21, as follows:

FIG. 22 illustrates one portion of the wiring substrate 2 as the print substrate in longitudinal section. Copper wirings 81A, 81B and 81C are formed on the front face of a glass epoxy resin substrate 80. Copper wirings 82A, 82B are formed on a rear face of the glass epoxy resin substrate 80. The copper wirings are covered and protected by a solder resist layer 84 except for a portion utilized in a connecting portion for mounting the multichip module 3 and the ASICs 4, 5, etc. In the illustrated example, the copper wiring 81A is connected to the copper wiring 82A through a through hole 83A, and the copper wiring 81C is connected to the copper wiring [82C] 82B through a through hole 83B, and a wiring situation using two wiring layers on the front and rear faces is schematically shown. However, this example is one example schematically showing the wiring structure. Various wiring patterns are actually formed in accordance with predetermined desirable wirings.

Please amend the paragraph bridging pages 32 and 33, from line 15 on page 32 to line 8 on page 33, as follows:

The SDAM has the matrix of a dynamic type memory cell in a memory cell array although this matrix is not particularly shown in FIGS. 6 and 7. Low active, column active reading, column active writing, refreshing operations, etc. are commanded by a command signal supplied in synchronization with a clock signal. The reading and writing operations are performed in synchronization with the clock signal by using an address signal supplied

together with the commands, or an address signal generated in an internal address counter. If a burst operation is commanded, data of a predetermined burst number can be continuously read or written. As illustrated in FIG. 7, the SDRAMs 12a to 12d have /CS (chip selection), /RAS (low address strobe), /CAS (column address strobe), /WE (write enable), [CLKE] CKE (clock enable), CLK (clock) and DQML, DQMH (data mask) as input terminals of an access control signal in addition to address input terminals A13 to A0 and data input/output terminals I/O15 to I/O0. DQML and DQMH (data mask) are control terminals for masking input data in a byte unit in a burst writing operation.

Please amend the paragraph bridging pages 49 and 50, from line 8 on page 49 to line 4 on page 50, as follows:

There is also the following power connecting mode although this mode is not shown in FIG. 13. For example, as shown in FIG. 13, there is also a case in which a power terminal or a ground terminal arranged in a semiconductor chip 11 cannot be linearly connected to a connecting terminal 15 (ground terminal) or a connecting terminal 15 (power 1 terminal) through a through hole. In this case, the connection is once made from the power terminal or the ground terminal arranged in the semiconductor chip 11 to a wiring layer 60A (ground layer) or 60D (~~ground~~ power 2 layer) formed within the core layer 60, or is once made from the power terminal or the ground terminal to a wiring layer 60B (power 1 layer) or a wiring layer 60C (~~power 2~~ ground layer). Thereafter, the connection is linearly made from the wiring layers 60A (ground layer), 60D (~~ground~~ power 2 layer), the wiring layer 60B (power 1 layer) and the wiring layer 60C (~~power 2~~ ground layer) corresponding to connectable portions of the corresponding connecting terminal 15 (ground terminal), connecting terminal 15 (power 1 terminal) or connecting terminal 15 (power 2 terminal) of the multichip module substrate 10

to the connecting terminal 15 (ground terminal), the connecting terminal 15 (power 1 terminal) or the connecting terminal 15 (power 2 terminal).

Please amend the paragraph on page 51, from lines 8 through 19, as follows:

A terminal 65 arranged in the semiconductor integrated circuit chip 64 and receiving the supply of the power electric potential (3.3 V) is connected to a solder bump electrode 15 as a power 1 terminal for receiving the supply of the power electric potential (3.3 V) through the wirings 61A, 61B, 61C arranged in the buildup layer 61 and the wirings 62A, 62B, 62C arranged in the buildup layer 62 although this construction is not shown in FIG. 20. The wiring layer 61C is electrically connected to the wiring layer 60B in a portion of the through hole TH formed in the core layer 60 so that the wiring layer 60B is set to a power 1 layer for receiving the supply of the power electric potential ~~(1.8 V)~~ (3.3 V).

Please amend the paragraph bridging pages 53 and 54, from line 11 on page 53 to line 2 on page 54, as follows:

As shown in FIG. 14C, an anisotropic electroconductive film 66 is stuck to the surface of the mounting pad 71. The anisotropic electroconductive film 66 is a thermosetting resin film in which electroconductive particulates such as nickel particles are dispersed and mixed into thermosetting resin. When force is applied to this anisotropic electroconductive film 66 in its thickness direction, the anisotropic electroconductive film 66 is elastically deformed as illustrated in FIG. 15, and the electroconductive particulates included in this deforming portion are chained and come in contact with each other so that electroconductivity is obtained only in this portion. This state is maintained by hardening the electroconductive particulates by heat and an adhesive action is also shown by this thermosetting property. The

size of the anisotropic electroconductive film [43] 66 stuck to the substrate may be determined in conformity with the size of a connected IC chip.